

# **ByteBlaster II Download Cable**

# **User Guide**



101 Innovation Drive San Jose, CA 95134 (408) 544-7000 http://www.altera.com

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# Contents

### Chapter 1. Setting Up the ByteBlaster II Download Cable

| Introduction  | . 1–1 |
|---|-------|
| Supported Devices   | . 1–1 |
| Power Requirements  | . 1–2 |
| Software Requirements   | . 1–2 |
| Hardware Setup  | . 1–2 |
| Software Setup  | . 1–3 |
| Installing the Driver on a Windows System                         | . 1–3 |
| Installing the Driver for Windows 2000 & Windows XP               | . 1–4 |
| Installing the Driver for Windows NT                              | . 1–5 |
| Installing the Driver on a Linux System                           | . 1–5 |
| Setting Up the ByteBlaster II Hardware in the Quartus II Software | . 1–7 |
|   |       |

### **Chapter 2. ByteBlaster II Specifications**

| ByteBlaster II Connections 2–1   Voltage Requirements 2–1 |
|---|
| Voltage Requirements                                      |
|   |
| Cable-to-Board Connection 2–2                             |
| ByteBlaster II 25-Pin Header Connection 2-3               |
| ByteBlaster II 10-Pin Header Connection 2-3               |
| Circuit Board Header Connection                           |
| Operating Conditions                                      |
| How to Contact Altera 2-8                                 |



# Chapter 1. Setting Up the ByteBlaster II Download Cable

## Introduction

The ByteBlaster<sup>™</sup> II download cable allows you to program and configure Altera<sup>®</sup> devices. This cable drives configuration data from a standard parallel printer port on your PC to the device on the printed circuit board (PCB). Because design changes are downloaded directly to the device, prototyping is easy and you can accomplish multiple design iterations in quick succession.

### **Supported Devices**

You can use the ByteBlaster II download cable to download configuration data to the following Altera<sup>®</sup> devices:

- Stratix<sup>®</sup> series FPGAs
- Cyclone<sup>™</sup> series FPGAs
- MAX<sup>®</sup> series CPLDs
- $\blacksquare \quad \text{APEX}^{^{\text{TM}}} \text{ series FPGAs}$
- ACEX<sup>®</sup> 1K FPGAs
- Mercury<sup>™</sup> FPGAs
- FLEX 10K<sup>®</sup> series FPGAs
- Excalibur<sup>™</sup> FPGAs

You can perform in-system programming of the following devices:

- Advanced configuration devices including EPC2, EPC4, EPC8, EPC16, and EPC1441 devices.
- Serial configuration devices including EPCS1, EPCS4, EPCS16, and EPCS64 devices.

In addition, you can perform SignalTap<sup>®</sup> II logic analysis.

The ByteBlaster II download cable supports target systems using 5.0 V TTL, 3.3 V LVTTL/LVCMOS, and single-ended I/O standards from 1.5 V to 3.3 V.

#### **Power Requirements**

The ByteBlaster II download cable requires between 1.5 V and 5.0 V from the target circuit board.

The ByteBlaster II cable can be used in 1.8-volt, 2.5-volt, 3.3-volt, and 5.0-volt systems.

The ByteBlaster II VCC (TRGT) pin must be connected to the appropriate voltage for the device being programmed. The pull-up resistors on the target circuit board for the configuration/programming signals must be connected to the same power supply as the ByteBlaster II  $V_{CC(TRGT)}$ .

### **Software Requirements**

The ByteBlaster II download cable is available for Windows 2000, Windows NT, Windows XP, and Linux.

Use the Quartus<sup>®</sup> II software version 4.0 or later to configure your device. The ByteBlaster II download cable also supports the following tools:

- Quartus II Programmer (for programming and configuration), which you can run within the Quartus II software or as a standalone version
- Quartus II SignalTap II Logic Analyzer (for logic analysis), which you can run within the Quartus II software or as a standalone version
- Nios<sup>®</sup> II IDE (for software downloading and debugging)
- Nios II IDE Flash Programmer (for programming Flash devices)

# Hardware Setup This section describes how to install and set up the ByteBlaster II download cable for device configuration and programming.

For plug and header dimensions, pin names, and operating conditions, see Chapter 2, "ByteBlaster II Specifications."

Connect your ByteBlaster II download cable to the circuit board as instructed below:

- 1. Disconnect the power cable from the circuit board.
- 2. Connect the ByteBlaster II cable to a parallel port on your PC.
- 3. Connect the ByteBlaster II download cable to the 10-pin header on the device board. Figure 1–1 on page 3 shows the ByteBlaster II download cable and the circuit board connector.



- 4. Connect the power cable to reapply power to the circuit board.
- If the Found New Hardware wizard opens prompting you to install a new hardware driver, close the wizard and install the hardware driver using the instructions provided in "Installing the Driver on a Windows System" or "Installing the Driver on a Linux System" depending on your system.

### **Software Setup** This section describes the following:

- Installing the Driver on a Windows System
- Installing the Driver on a Linux System
- Setting Up the ByteBlaster II Hardware in the Quartus II Software

#### Installing the Driver on a Windows System

This section describes how to install the ByteBlaster II driver on a Windows system.

Before you begin the installation, verify the ByteBlaster II driver is located in your directory:

\<Quartus II system directory>\drivers\win2000\win2000.inf

# If the driver is not in your directory, download the ByteBlaster II driver from the Altera web site: www.altera.com/support/software/drivers/

#### Installing the Driver for Windows 2000 & Windows XP

To install the driver for Window 2000 or Windows XP, follow the directions below:

 For Window 2000, choose Settings > Control Panel (Windows Start menu).

or

For Windows XP, choose Control Panel (Windows Start menu).

- 2. Click Switch to Classic View if necessary (Control Panel window).
- 3. Double-click the **Add Hardware** icon to start the **Add Hardware** wizard and click **Next** to continue.
- 4. Select Yes, I have already connected the hardware and click Next.
- 5. Select **Add a new hardware device** from the **Installed hardware** list, and click **Next** to continue.
- 6. Select **Install from a list or specified location (Advanced)** and click **Next** to continue.
  - Depending on your system, the wording of this option may vary slightly.
- 7. Select **Sound**, **video** and **game controllers**, and click **Next** to continue.
- Select Have Disk and browse to the location of the driver on your system. The default location is the \<Quartus II system directory>\ drivers\win2000 directory.
- 9. Select win2000.inf and click Open to continue.
- 10. Click **OK** to install the selected driver.
- 11. Click **Continue Anyway** when the Software Installation warning appears.
- 12. Select Altera ByteBlaster and click Next to continue.

- 13. Click **Next** to install the driver.
- 14. Click **Continue Anyway** when the Hardware Installation warning appears.
- 15. Click **Finish** in the Completing the Add Hardware Wizard window. Reboot your system.

#### Installing the Driver for Windows NT

To install the driver for Window NT, follow the directions below:

- For Window NT, choose Settings > Control Panel (Windows Start menu).
- 2. Double-click the Multimedia icon in the Control Panel window.
- 3. Click the **Devices** tab and click the **Add** button.
- 4. Click **Unlisted or Updated Driver** from the **List of Drivers** list box and click **OK**.
- 5. Browse to the location of the driver on your system. The default location is the \<*Quartus II system directory*>\ drivers\win2000 directory. Click OK.
- 6. Select **Altera ByteBlaster** or **Altera ByteBlaster II** in the **Add Unlisted or Updated Driver** window and click **OK**. Reboot your system.

#### Installing the Driver on a Linux System

The Altera ByteBlaster kernel driver is required for Linux workstations running Red Hat Linux version 7.3 or 8.0 or Red Hat Enterprise Linux 3.0 that use the ByteBlaster II download cable. You must install and compile the Altera ByteBlaster kernel driver separately from the Quartus II software.

To compile the Altera ByteBlaster kernel driver, you must have the following Red Hat Package Manager (RPM) packages, which are available from the Red Hat web site at **www.redhat.com**:

- .gcc-2.96-81
- .make-3.79.1-5
- binutils-2.10.91.0.2-3
- kernel-headers (RPM version must correspond to kernel version)

To verify that an RPM is installed, use the rpm -q <*name*> + command. For example, rpm -q gcc + verifies that the gcc RPM is installed.

You do not need to install the ByteBlaster II download cable before installing the Altera ByteBlaster kernel driver.

You must have superuser or "root" privileges to install this driver.

To install the driver for Linux, follow the directions below:

1. Decompress the **byteblaster.tar.gz** file by typing the following command at the command prompt:

tar -xzvf byteblaster.tar.gz 🕶

2. Access the new directory by typing the following command at the command prompt:

cd byteblaster 🕶

3. Run the **configure** install script by typing the following command at the command prompt:

./configure ←

4. Compile the Altera ByteBlaster kernel driver by typing the following command at the command prompt:

make 🖊

5. Become root and compile the Altera ByteBlaster kernel driver module and device nodes by typing the following command at the command prompt:

make install 🕂

6. To install the Altera ByteBlaster kernel driver, type the following command at the command prompt:

jtagconfig --add byteblaster2 /dev/byteblaster0 🛩

7. To determine whether the ByteBlaster II download cable and the Altera ByteBlaster kernel driver were installed correctly, display a list of available devices by the typing the following commands at the command prompt:

jtagconfig 🛩

You should see a list of devices on your JTAG chain, including the ByteBlaster II download cable.

#### Setting Up the ByteBlaster II Hardware in the Quartus II Software

Use the following steps to set up the ByteBlaster II hardware in the Quartus II software:

- 1. Start the Quartus II software.
- 2. Choose Programmer (Tools menu).
- 3. Click **Hardware Setup**. The **Hardware Settings** tab of the **Hardware Setup** dialog box is displayed.
- 4. Click Add Hardware. The Add Hardware dialog box is displayed. Select ByteBlaster MV or ByteBlaster II and click OK.
- 5. **ByteBlasterII** is now visible in the **Available hardware items** list of the **Hardware Setup** dialog box, as shown in Figure 1–2.

Figure 1–2. Hardware Setup Dialog Box

| Hardware Setup  |                  |              |                                 |  |  |  |  |
|---|------------------|--------------|---------------------------------|--|--|--|--|
| Hardware Settings JTAG Settings<br>Select a programming hardware setup to use when programming devices. This programming<br>hardware setup applies only to the current programmer window. |                  |              |                                 |  |  |  |  |
| Currently selected hardware:  | ByteBlasterII [[ | .PT1]        |                                 |  |  |  |  |
| Hardware<br>ByteBlasterII   | Server<br>Local  | Port<br>LPT1 | Add Hardware<br>Remove Hardware |  |  |  |  |
|   |                  |              | Close                           |  |  |  |  |

- 6. Click **Close** to close the **Hardware Setup** dialog box.
- In the Mode list, select the desired mode (Programmer window). Table 1–1 describes each mode.
- The ByteBlaster II supports the Joint Test Action Group (JTAG), Passive Serial Programming, and Active Serial modes.

| Table 1–1. Programming Modes   |  |  |  |  |
|--------------------------------|--|--|--|--|
| Mode                           | Mode Description   |  |  |  |
| Joint Test Action Group (JTAG) | Programs or configures all Altera devices supported by the Quartus II software, excluding FLEX 6000 devices. |  |  |  |
| In-Socket Programming          | Not supported by the ByteBlaster II cable.   |  |  |  |
| Passive Serial Programming     | Configures all Altera devices supported by the Quartus II software, excluding MAX 3000 and MAX 7000 devices. |  |  |  |
| Active Serial Programming      | Programs a single EPCS1, EPCS4, EPCS16, or EPCS64 serial configuration device.                               |  |  |  |

••••

For details about programming devices and creating secondary programming files, see the "Programming & Configuration" chapter of the *Introduction to Quartus II Handbook*.

For further information, see the Programming module of the Quartus II online tutorial.

For further information, refer to the following topics in the Quartus II online Help:

- Changing the Hardware Setup
- Programmer Introduction
- Overview: Working with Chain Description Files
- Overview: Converting Programming Files



# Chapter 2. ByteBlaster II Specifications

## **Overview**

This chapter provides comprehensive information about the ByteBlaster<sup>™</sup> II download cable, including the following:

- ByteBlaster II connections
  - Voltage requirements
  - Cable-to-board connection
  - ByteBlaster II 25-pin header connection
  - ByteBlaster II 10-pin header connection
  - Circuit board header connection
- Operating conditions

# ByteBlaster II Connections

The ByteBlaster II cable has a 25-pin male header parallel printer plug that connects to the PC, and a 10-pin female plug that connects to the circuit board. Data is downloaded from the parallel printer port on the PC through the ByteBlaster II cable to the circuit board.

### **Voltage Requirements**

The ByteBlaster II V<sub>CC(TRGT)</sub> pin must be connected to a specific voltage for the device being programmed. Connect pull-up resistors to the same power supply as the ByteBlaster II V<sub>CC(TRGT)</sub>. See Table 2–1 for voltage requirements for specific device families.

| Table 2–1. ByteBlaster II V <sub>CC(TRGT)</sub> Pin Voltage Requirements | (Part 1 of 2)                        |
|--|--------------------------------------|
| Device Family  | ByteBlaster II VCC Voltage Required  |
| MAX II devices   | As specified by $V_{CCIO}$ of Bank 1 |
| MAX 7000S devices  | 5 V                                  |
| MAX 7000AE and MAX 3000A devices   | 3.3 V                                |
| MAX 7000B device   | 2.5 V                                |
| Stratix II, Stratix GX, and Stratix devices                              | As specified by V <sub>CCSEL</sub>   |
| Cyclone II, Cyclone, APEX II, APEX 20K, and Mercury devices              | As specified by $V_{CCIO}$           |
| FLEX 10K, FLEX 8000, and FLEX 6000 devices                               | 5 V                                  |
| FLEX 10KE devices  | 2.5 V                                |
| FLEX 10KA and FLEX 6000A devices   | 3.3 V                                |

| Table 2–1. ByteBlaster II $V_{CC(TRGT)}$ Pin Voltage Requirements | (Part 2 of 2) |
|---|---------------|
| EPC2 and EPC1441 devices  | 5 V or 3.3 V  |
| EPC4, EPC8, and EPC16 devices                                     | 3.3 V         |
| EPCS1, EPCS4, EPCS16, and EPCS64 devices                          | 3.3 V         |

### **Cable-to-Board Connection**

The ByteBlaster II cable has a standard parallel printer plug that connects to the PC. Figure 2–1 shows a block diagram of the ByteBlaster II download cable.





### ByteBlaster II 25-Pin Header Connection

The 25-pin male header connects to a parallel port with a standard parallel cable. Table 2–2 identifies the plug pin names and the corresponding programming modes.

| Table 2–2. ByteBlaster II 25-Pin Header Pin-Outs |                |   |                |                       |                |                               |  |
|--|----------------|---|----------------|-----------------------|----------------|-------------------------------|--|
| Din  | AS Mode        |   | PS Mode        |                       | JTAG Mode      |                               |  |
| FIII   | Signal Name    | Description                             | Signal Name    | Description           | Signal Name    | Description                   |  |
| 2  | DCLK           | Clock signal                            | DCLK           | Clock signal          | TCK            | Clock signal                  |  |
| 3  | nCONFIG        | Configuration control                   | nCONFIG        | Configuration control | TMS            | JTAG state<br>machine control |  |
| 4  | nCS            | Serial configuration device chip select | —              | No connect            |                | No connect                    |  |
| 5  | nCE            | Cyclone chip<br>enable                  | —              | No connect            |                | No connect                    |  |
| 8  | ASDI           | Active serial data in                   | DATA0          | Data to device        | TDI            | Data to device                |  |
| 11   | CONF_DONE      | Configuration done                      | CONF_DONE      | Configuration done    | TDO            | Data from device              |  |
| 13   | DATAOUT        | Active serial data out                  | nSTATUS        | Signal status         |                | No connect                    |  |
| 15   | nVCC<br>Detect |   | nVCC<br>Detect |                       | nVCC<br>Detect |                               |  |
| 18 to 25   | GND            | Signal ground                           | GND            | Signal ground         | GND            | Signal ground                 |  |

### **ByteBlaster II 10-Pin Header Connection**

The 10-pin female plug connects to a 10-pin male header on the circuit board. Figure 2–2 shows the dimensions of the female plug.



Figure 2–2. ByteBlaster II 10-Pin Female Plug Dimensions

Table 2–3 identifies the 10-pin female plug signal names and the corresponding programming mode.

| Tal  | Table 2–3. ByteBlaster II Female Plug Signal Names & Programming Modes |   |                 |                       |             |                               |  |
|------|--|---|-----------------|-----------------------|-------------|-------------------------------|--|
| Din  | AS Mode  |   | AS Mode PS Mode |                       | JTAG Mode   |                               |  |
| FIII | Signal Name  | Description                             | Signal Name     | Description           | Signal Name | Description                   |  |
| 1    | DCLK   | Clock signal                            | DCLK            | Clock signal          | TCK         | Clock signal                  |  |
| 2    | GND  | Signal ground                           | GND             | Signal ground         | GND         | Signal ground                 |  |
| 3    | CONF_DONE  | Configuration done                      | CONF_DONE       | Configuration done    | TDO         | Data from device              |  |
| 4    | VCC (TRGT)   | Target power supply                     | VCC (TRGT)      | Target power supply   | VCC (TRGT)  | Target power supply           |  |
| 5    | nCONFIG  | Configuration control                   | nCONFIG         | Configuration control | TMS         | JTAG state<br>machine control |  |
| 6    | nCE  | Cyclone chip<br>enable                  | —               | No connect            | —           | No connect                    |  |
| 7    | DATAOUT  | Active serial data out                  | nSTATUS         | Configuration status  | —           | No connect                    |  |
| 8    | nCS  | Serial configuration device chip select | _               | No connect            | _           | No connect                    |  |
| 9    | ASDI   | Active serial data in                   | DATA0           | Data to device        | TDI         | Data to device                |  |
| 10   | GND  | Signal ground                           | GND             | Signal ground         | GND         | Signal ground                 |  |

The circuit board must supply  $V_{CC(TRGT)}$  and ground to the ByteBlaster II cable for the I/O drivers.

#### **Circuit Board Header Connection**

The circuit board's 10-pin male header has two rows of five pins. connected to the device's programming or configuration pins. Figure 2–3 shows the dimensions of a typical 10-pin male header.





# Operating Conditions

Tables 2–4 through 2–6 summarize the maximum ratings, recommended operating conditions, and DC operating conditions for the ByteBlaster II cable.

| Table 2–4. ByteBlaster II Cable Absolute Maximum Ratings |                       |                         |       |      |      |  |
|--|-----------------------|-------------------------|-------|------|------|--|
| Symbol   | Parameter             | Conditions              | Min   | Max  | Unit |  |
| V <sub>CC(TRGT)</sub>                                    | Target supply voltage | With respect to ground  | -0.3  | 5.5  | V    |  |
| I <sub>I</sub>   | Input current         | TDO <b>or</b> dataout   | -10.0 | 10.0 | mA   |  |
| I <sub>o</sub>   | Output current        | TCK, TMS, TDI, nCS, nCE | -20.0 | 20.0 | mA   |  |

| Table 2–5. ByteBlaster II Cable Recommended Operating Conditions |   |  |       |      |   |  |  |
|--|---|--|-------|------|---|--|--|
| Symbol   | ol Parameter Conditions Min Ma              |  |       |      |   |  |  |
| V <sub>CC(TRGT)</sub>  | Target supply voltage, 5.0-V operation      |  | 4.75  | 5.25 | V |  |  |
|  | Target supply voltage, 3.3-V operation3.0   |  | 3.0   | 3.6  | V |  |  |
|  | Target supply voltage, 2.5-V operation2.375 |  | 2.625 | V    |   |  |  |
|  | Target supply voltage, 1.8-V operation      |  | 1.71  | 1.89 | V |  |  |
|  | Target supply voltage, 1.5-V operation      |  | 1.43  | 1.57 | V |  |  |

| Table 2–6. ByteBlaster II Cable DC Operating Conditions |                                 |   |                            |       |      |  |
|---|---------------------------------|---|----------------------------|-------|------|--|
| Symbol  | Parameter                       | Conditions  | Min                        | Max   | Unit |  |
| V <sub>IH</sub>   | High-level input voltage        |   | V <sub>CC(TRGT)</sub> -0.2 |       | V    |  |
| V <sub>IL</sub>   | Low-level input voltage         |   |                            | 0.15  | V    |  |
| V <sub>OH</sub>   | 5.0-V high-level output voltage | $V_{CC(TRGT)} = 4.5 \text{ V}, \text{ I}_{OH} = 8 \text{ mA}$ | 4.4                        |       | V    |  |
|   | 3.3-V high-level output voltage | $V_{CC(TRGT)} = 3.0 \text{ V}, \text{ I}_{OH} = 4 \text{ mA}$ | 2.9                        |       | V    |  |
|   | 2.5-V high-level output voltage | $V_{CC(TRGT)}$ = 2.375 V, $I_{OH}$ = 2 mA                     | 2.275                      |       | V    |  |
|   | 1.8-V high-level output voltage | $V_{CC(TRGT)} = 1.71 \text{ V}, I_{OH} = 2 \text{ mA}$        | 1.61                       |       | V    |  |
|   | 1.5-V high-level output voltage | $V_{CC(TRGT)} = 1.43 \text{ V}, \text{ IOH} = 2 \text{ mA}$   | 1.33                       |       | V    |  |
| V <sub>OL</sub>   | 5.0-V low-level output voltage  | $V_{CC(TRGT)} = 5.5 \text{ V}, \text{ I}_{OL} = 8 \text{ mA}$ |                            | 0.125 | V    |  |
|   | 3.3-V low-level output voltage  | $V_{CC(TRGT)} = 3.6 \text{ V}, \text{ I}_{OL} = 4 \text{ mA}$ |                            | 0.125 | V    |  |
|   | 2.5-V low-level output voltage  | $V_{CC(TRGT)}$ = 2.625 V, $I_{OL}$ = 2 mA                     |                            | 0.125 | V    |  |
|   | 1.8-V low-level output voltage  | $V_{CC(TRGT)} = 1.89 \text{ V}, I_{OL} = 2 \text{ mA}$        |                            | 0.125 | V    |  |
|   | 1.5-V low-level output voltage  | $V_{CC(TRGT)} = 1.57 \text{ V}, \text{ IOL} = 2 \text{ mA}$   |                            | 0.125 | V    |  |
| I <sub>CC(USB)</sub>                                    | Operating current (No Load)     | (Typical I <sub>CC</sub> = 80 mA)                             |                            | 150   | mA   |  |

## **References** For more infor

For more information on configuration and in-system programmability (ISP), see the following sources:

- AN 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices
- AN 95: In-System Programmability in MAX Devices
- "Configuring Cyclone FPGAs" chapter in the Cyclone Device Handbook
- Configuring Cyclone II Devices" chapter in the *Cyclone II Device Handbook*
- Configuring Stratix II Devices" chapter in Volume 2 of the *Stratix II Device Handbook*
- Configuring Stratix and Stratix GX Devices" chapter in the *Stratix Device Handbook*
- "In-System Programmability Guidelines for MAX II Devices" chapter in the MAX II Device Handbook
- Serial Configuration Devices Data Sheet
- "Programming & Configuration" chapter in the Introduction to Quartus II manual
- The Programming module of the Quartus II online tutorial
- Refer to the following glossary definitions in Quartus II Help:
  - "ByteBlaster II Cable" (general description)
  - "Configuration scheme" (general description)
  - "Programming files" (general description)
  - Refer to the following procedures in Quartus II Help:
    - Programming a Single Device or Multiple Devices in JTAG or Passive Serial Mode
    - Programming a Single Device in Active Serial Programming Mode
    - Selecting the Communications Cable for the SignalTap II Logic Analyzer
- Refer to the following introduction and overview topics in Quartus II Help:
  - Programmer Introduction
  - Overview: Working with Chain Description Files
  - Overview: Converting Programming Files

## **Revision History** The table below shows the revision history of this user guide.

| Chapter | Date          | Version | Changes Made    |
|---------|---------------|---------|-----------------|
| All     | December 2004 | 1.1     | Re-release      |
| All     | July 2004     | 1.0     | Initial release |

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